Docket No.: 0020-5383 PUS1

(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Hiroshi IWATA et al.	Confirmation No.:8857
Application No.: 10/540,019	Art Unit: 2814
Filed: June 22, 2005	Examiner: L. Pham
For: SEMICONDUCTOR STORAGE DEVICE AND PORTABLE ELECTRONIC EQUIPMENT	

VERIFICATION OF ENGLISH TRANSLATION

MS Amendment
Commissioner for Patents
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Dear Sir:

I, Hiroshi Yamazaki, of c/o IMP Building, 1-3-7, Shiromi, Chuo-ku, Osaka 540-0001 Japan, declare that I am conversant in both the Japanese and English languages and that the English translation as attached hereto is accurate translation of Japanese Patent Application No. 2002-379737 filed December 27, 2002.

Signed this 5th day of November, 2008

Hiroshi YAMAZAKI

JAPAN PATENT OFFICE

This is to certify that the annexed is a true copy of the following application as filed with this Office.

Date of Application: December 27, 2002

Application Number: Patent Application No. JP2002-379737

Applicant: SHARP KABUSHIKI KAISHA

Commissioner,

Japan Patent Office

(Seal)

Document Name:	Application for Patent
Docket No.:	02J05058
Date of Application:	December 27, 2002
Addressee:	Commissioner, Patent Office
International Patent Classification:	H01L 27/10
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Payment of Fees:

Prepayment Book No.: 012313
Amount to be paid: ¥21,000

Attached Document:

Item:	Specification	1 copy
Item:	Drawings	1 copy
Item:	Abstract	1 copy
Registration No. of General Power:	9703283	
Registration No. of General Power:	9703284	

Request for Proof Transmission: Yes

Document name: Claims

1. A semiconductor storage device comprising:

a single gate electrode formed on a semiconductor layer, with a gate insulation film disposed therebetween;

a channel region arranged under the gate electrode;

diffusion regions arranged on opposite sides of the channel region; and

memory function bodies formed at least on opposite sides of the gate electrode and having a function to retain electric charges.

2. A semiconductor storage device comprising a plurality of memory elements that are arranged, each memory element comprising:

a word line formed on a semiconductor layer via a gate insulation film;

a channel region arranged under the word line;

diffusion regions arranged on opposite sides of the channel region; and

memory function bodies formed at least on opposite sides of the word line and having a function to retain electric charges, each of the memory function bodies existing over part of the channel region and the corresponding part of each of the diffusion regions,

straddling a boundary therebetween, wherein

the plurality of memory elements sharing the word line share the memory function bodies formed on the opposite sides of the word line.

3. A semiconductor storage device comprising a plurality of memory elements that are arranged sharing a single word line, each memory element comprising:

the single word line formed on a semiconductor layer via a gate insulation film;

a channel region arranged under the single word line;

diffusion regions arranged on opposite sides of the channel region;

memory function bodies formed only on both sides of the word line and having a function to retain electric charges, each of the memory function bodies existing over part of the channel region and the corresponding part of each of the diffusion regions, straddling a boundary therebetween, wherein

the memory function body is formed of an insulation material, and the plurality of memory elements sharing the one word line share the memory function bodies formed on the opposite sides of the word line.

4. The semiconductor storage device as claimed in claim 3, wherein a word line to be selected when

information is rewritten to the memory element is only the single word line.

5. A semiconductor storage device comprising:

a single gate electrode formed on a semiconductor layer, with a gate insulation film disposed therebetween;

a channel region arranged under the gate electrode;

diffusion regions arranged on opposite sides of the channel region; and

memory function bodies formed at least on opposite side walls of the gate electrode and having a function to retain electric charges, wherein

the memory function bodyies are each comprised of an insulative material, and

at least part of each memory function body is formed so as to overlap with part of the corresponding diffusion region.

6. The semiconductor storage device as claimed in any one of claims 1 through 5, wherein the semiconductor layer is comprised of a SOI layer.

7. The semiconductor storage device as claimed in any one of claims 1 through 5, wherein the semiconductor layer includes a well region.

8. The semiconductor storage device as claimed in

any one of claims 1 through 5, wherein each of the memory function bodies includes a charge retention film having a function of storing electric charges, and an insulation film.

9. The semiconductor storage device as claimed in claim 8, wherein the memory function body includes a charge retention film that has a surface roughly parallel to a surface of the gate insulation film.

10. The semiconductor storage device as claimed in claim 9, wherein the memory function body includes a charge retention film extended roughly parallel to a side surface of the gate electrode or the word line.

11. The semiconductor storage device as claimed in claim 10, wherein the memory function body further includes an insulation film that separates the gate electrode or the word line from the second portion of the charge retention film extended roughly parallel to the side surface of the gate electrode or the word line.

12. The semiconductor storage device as claimed in any one of claims 9 through 11, wherein the memory function body further includes an insulation film that separates the charge retention film from the channel region or the semiconductor layer.

13. The semiconductor storage device as claimed in claim 12, wherein the insulation film that separates the

the charge retention film from the channel region or the semiconductor layer has a film thickness, which is smaller than a film thickness of the gate insulation film and not smaller than 0.8 nm.

14. The semiconductor storage device as claimed in claim 12, wherein the insulation film that separates the charge retention film from the channel region or the semiconductor layer has a film thickness, which is greater than a film thickness of the gate insulation film and not greater than 20 nm.

15. Portable electronic equipment having the semiconductor storage device as claimed in any one of claims 1 through 14.

Document name: Specification

Title of the invention: SEMICONDUCTOR STORAGE DEVICE AND PORTABLE ELECTRONIC EQUIPMENT

Technical field:

[0001]

The present invention relates to a semiconductor storage device and portable electronic equipment. More particularly, the present invention relates to a semiconductor storage device in which field-effect transistors having memory function parts are arrayed, each function part having a function of holding electric charges or polarization, and portable electronic equipment that employs such a semiconductor storage device.

Background art:

[0002]

The following will describe a flash memory as a representative example of conventional nonvolatile memories. Fig. 21 is a schematic sectional view of an example of a flash memory cell. In Fig. 21, the reference numerals 901, 902, 903, 904, 905, 906 and 907 respectively denote a semiconductor substrate, a floating gate, a word line (control gate), a diffusion layer source line, a diffusion layer bit line, element isolation regions and an insulation film.

[0003]

The flash memory cell includes a floating gate, and retains storage as the quantity of charge in the floating gate. In the memory cell array constructed by arranging the memory cells, the desired memory cell can be subjected to rewrite and read operations by selecting the specified word line and bit line and applying a prescribed voltage to the lines.

[0004]

Fig. 22 schematically shows a drain current (Id) vs. gate voltage (Vg) characteristic when the quantity of charges in the floating gate 902 changes. As the quantity of charges in the floating gate increases, the threshold voltage increases, and the Id-Vg curve is displaced roughly parallel in a direction in which the gate voltage Vg increases.

[0005]

Problem to be solved by the invention:

However, in the aforementioned conventional flash memory that has the floating gate between the word line (gate electrode) and the channel region, because it is necessary to prevent leakage of electric charges from the floating gate 902, it has been difficult to reduce the thickness of an insulation film that isolates the floating gate from the word line and an insulation film that isolate the floating gate from the channel region. Therefore, it

has been difficult to reduce the thickness of a practically gate insulation film, and this has hindered the miniaturization of the memory cell.

[0006]

The present invention was made in view of the above problem, and an object of the present invention is to provide a nonvolatile memory that is easy to miniaturize.

Means of solving the problem:

[0007]

Means of solving the problem:

In order to accomplish the above object, a semiconductor storage device according to a first invention includes:

a single gate electrode formed on a semiconductor layer, with a gate insulation film disposed therebetween;

a channel region arranged under the gate electrode;

diffusion regions arranged on opposite sides of the channel region; and

memory function bodies formed at least on opposite sides of the gate electrode and having a function to retain electric charges.

[0008]

According to the above arrangement, the memory

function bodies are formed independently of the gate insulating film and provided on both sides of the gate electrode. Thus, the device is able to perform a two-bit operation. Furthermore, because the memory function bodies are separated from each other by the gate electrode, interference during rewrite can effectively be prevented. Further, because the gate insulating film is independent of the memory function bodies, the gate insulating film is made thinner, so that short channel effect can be easily prevented. Thus, further miniaturization of a memory element is facilitated.

[0009]

A semiconductor storage device according to a second invention includes a plurality of memory elements that are arranged, each memory element comprising:

a word line formed on a semiconductor layer via a gate insulation film;

a channel region arranged under the word line;

diffusion regions arranged on opposite sides of the channel region; and

memory function bodies formed at least on opposite sides of the word line and having a function to retain electric charges, each of the memory function bodies existing over part of the channel region and the corresponding part of each of the diffusion regions,

straddling a boundary therebetween, wherein

the plurality of memory elements sharing the word line share the memory function bodies formed on the opposite sides of the word line.

[0010]

This arrangement corresponds to an embodiment of an array of a plurality of the semiconductor storage devices according to the first invention. Therefore, miniaturization of the semiconductor storage device comprising the array of the memory elements is easier.

[0011]

A semiconductor storage device according to a third invention includes a plurality of memory elements that are arranged sharing a single word line, each memory element comprising:

the single word line formed on a semiconductor layer via a gate insulation film;

a channel region arranged under the single word line;

diffusion regions arranged on opposite sides of the channel region;

memory function bodies formed only on both sides of the word line and having a function to retain electric charges, each of the memory function bodies existing over part of the channel region and the

corresponding part of each of the diffusion regions, straddling a boundary therebetween, wherein
the memory function body is formed of an insulation material, and the plurality of memory elements sharing the one word line share the memory function bodies formed on the opposite sides of the word line.

[0012]

This arrangement also corresponds to an embodiment of an array of a plurality of the semiconductor storage devices according to the first invention. Further, the memory function bodies are formed of one or more insulative materials and arranged only on both sides of the single word line. Therefore, the fabrication process for the semiconductor stsorage device having the memory elements arrayed is simplified, which in turn provides improved yields. Further, miniaturization of the memory elements is easier, so that the scale of integration will be increased. In addition, the write operation is well performed.

[0013]

In one embodiment, a word line to be selected when information is rewritten to the memory element is only the single word line.

[0014]

In the embodiment, the number of word lines

that are required for the memory operations is made minimum. Thus, a memory cell array can be packed at a higher density.

[0015]

A semiconductor storage device according to a fourth embodiment includes:

a single gate electrode formed on a semiconductor layer, with a gate insulation film disposed therebetween;

a channel region arranged under the gate electrode;

diffusion regions arranged on opposite sides of the channel region; and

memory function bodies formed at least on opposite side walls of the gate electrode and having a function to retain electric charges, wherein

the memory function bodyies are each comprised of an insulative material, and

at least part of each memory function body is formed so as to overlap with part of the corresponding diffusion region.

[0016]

In the embodiment, the memory function bodies are comprised of one or more insulative materials and formed on both sides of the single gate electrode such that at least part of each memory function body overlaps with

part of the corresponding diffusion region. This arrangement can simplify the memory element fabrication process and thus increase yields. Further, miniaturization of the memory elements is easier, and the write operation to the memory elements is well performed.

[0017]

In one embodiment, the semiconductor layer is comprised of a SOI layer.

[0018]

In this embodiment, junction capacitance between the diffusion regions and a body region is markedly reduced, which enables the increase of the operation speed of the memory elements and the reduction of power consumption.

[0019]

In one embodiment, the semiconductor layer includes a well region.

[0020]

In the embodiment, it is easy to controll electric characteristics (breakdown voltage, junction capacitance, short-channel effect), with the impurity concentration in an area right under the gate insulation film being made optimum in view of the memory operations (rewrite operations and read operations).

[0021]

In one embodiment, each of the memory function bodies includes a charge retention film having a function of storing electric charges, and an insulation film.

[0022]

In this embodiment, it is possible to prevent dissipation of electric charges and improve the memory retention characteristic. Also, it is possible to properly reduce the volume of the charge retention film, as compared with a case in which the memory function body consists of the charge retention film only. Further, the proper reduction of the volume of the charge retention film can restrain migration of the electric charges within the charge retention film, thus suppressing a change in characteristics due to the migration of the charges during the memory retention. Thus, an improved memory retention characteristic is achieved.

[0023]

In one embodiment, the memory function body includes a charge retention film that has a surface roughly parallel to a surface of the gate insulation film.

[0024]

In the embodiment, it is possible to effectively control easiness of formation of an inversion layer in the offset region with use of an amount of electric charges stored in the charge retention film,

thereby enabling increase of memory effect. Because the charge retention film is substantially parallel to the surface of the gate insulation film, change of memory effect may be kept relatively small even with a dispersed offset amount, enabling restraint of memory effect dispersion. In addition, because the charge retention film is in the shape of a film substantially parallel to the surface of the gate insulation film, upward movement of electric charges is suppressed, and therefore change of characteristics due to the movement of electric charges during memory holding is restrained. Thus, it is possible to obtain a semiconductor storage device having good charge holding characteristics wherein the memory effect is large and less varied.

[0025]

In one embodiment, the memory function body includes a charge retention film extended roughly parallel to a side surface of the gate electrode or the word line.

[0026]

In this embodiment, the holding characteristic of the device is prevented from deterioration, and at the same time, the rewriting speed can be increased.

In one embodiment, the memory function body further includes an insulation film that separates the gate electrode or the word line from the charge retention film

extended roughly parallel to the side surface of the gate electrode or the word line.

[0027]

In this embodiment, movement of the electric charges between the gate electrode and the charge retention film extended roughly parallel to the gate electrode side surface is suppressed. Thus, reliability of the semiconductor storage device increases.

[0028]

In one embodiment, the memory function body further includes an insulation film that separates the charge retention film including a surface roughly parallel to the surface of the gate insulating film from the channel region or the semiconductor layer.

[0029]

In this embodiment, dissipation of charges from the first portion of the charge retention film is suppressed. Therefore, a semiconductor storage device with better holding characteristics is obtainable.

[0030]

In one embodiment, the insulation film that separates the the charge retention film from the channel region or the semiconductor layer has a film thickness, which is smaller than a film thickness of the gate insulation film and not smaller than 0.8 nm.

[0031]

In this embodiment, without deteriorating the voltage withstanding performance or electric strength of the memory, reduction of voltage in the write operation and erase operation or implementing a high-speed write operation and erase operation is enabled. This makes it possible to increase memory effect.

[0032]

In one embodiment, the insulation film that separates the charge retention film from the channel region or the semiconductor layer has a film thickness, which is greater than a film thickness of the gate insulation film and not greater than 20 nm.

[0033]

In this embodiment, it is possible to improve the holding characteristics without deteriorating the memory short channel effect.

[0034]

Portable electronic equipment according to a fifth invention includes the semiconductor storage device of the present invention.

[0035]

As described above, since the semiconductor storage device that facilitates the fabricating process for the memory section and the logic circuit section in

combination, and that allows a high speed read operation, is employed for the portable electronic equipment, it is possible to improve the operating speed of the portable electronic equipment, and reduce the production costs.

[0036]

Mode for carrying out the invention:

An outline of a memory element to be employed in the semiconductor storage device of the present invention will be described first.

[0037]

The memory element employed in the semiconductor storage device of the present invention is constructed mainly of first conductivity type regions that are diffusion regions, a second conductivity type region, memory function bodies each straddling the border between the first and second conductivity type regions, and an electrode on an insulation film, or mainly of a gate insulation film, a gate electrode on the gate insulation film, memory function bodies on both sides of the gate electrode, source/drain regions (diffusion regions) respectively formed on opposite sides of the gate electrode of the memory function bodies, and a channel region under the gate electrode.

[0038]

The memory element functions as a memory device

storing four-valued or more information by storing binary or more information in one charge retention film. The memory element also functions as a memory cell having a selector transistor function and a memory transistor function because of the variable resistance effect of the memory function body. However, the memory element does not necessarily need to store four-valued or more information, but it may also function to store, for example, binary information.

[0039]

It is preferable that the semiconductor storage device of the present invention is formed on a semiconductor substrate, preferably in a first conductivity type well region formed in the semiconductor substrate.

[0040]

The semiconductor substrate is not limited to particular ones as far as it is applicable to semiconductor apparatuses, and it is possible to use various substrates such as bulk substrates made from elemental semiconductors such as silicon and germanium, or compound semiconductors such as SiGe, GaAs, InGaAs, ZnSe, and GaN; SOI (Silicon on Insulator) substrates; SOS (Silicon on Sapphire) substrates, and multilayer SOI substrates, and substrates having a semiconductor layer on a glass or plastic substrate. Among others, a silicon substrate or an SOI substrate having a

silicon layer formed as a surface semiconductor layer is preferable. The semiconductor substrate or the semiconductor layer may be monocrystal (e.g., a single crystal obtained by epitaxial growth), polycrystalline, or amorphous, though a current amount flowing inside will be slightly different among them.

[0041]

On the semiconductor substrate or semiconductor layer, it is preferable that device isolation regions are formed. Elements such as transistors, capacitors and resistors, circuits composed of such elements, semiconductor devices, and an inter-layer insulating film or films may be formed in combination in a single or a multilayer structure on the semiconductor substrate or the semiconductor layer. It is noted that the device isolation regions may be formed by any of various device isolation films including a LOCOS film, a trench oxide film, and an STI film. The semiconductor substrate may be either of a P type or an N type conductivity type, and it is preferable that at least one first conductivity type (P type or N type) well region is formed in the semiconductor substrate. Acceptable impurity concentrations of the semiconductor layer and the well region are those within the range known in the art. It is noted that in the case of using an SOI substrate as the semiconductor substrate, a well region may

be formed in the surface semiconductor layer, and also a body region may be provided under the channel region.

[0042]

Materials of the gate insulating film or the insulation film are not particularly limi0ted as far as they are usable in typical semiconductor apparatuses. For example, insulating films including a silicon oxide film and a silicon nitride film, and high-dielectric films including aluminum oxide films, titanium oxide films, tantalum oxide films, hafnium oxide films are usable in the form of a single-layer film or a multi-layer film. Among others, the silicon oxide film is preferable. An appropriate thickness of the gate insulating film is, for example, approx. 1 to 20 nm, preferably 1 to 6 nm. The gate insulating film may be only formed right under the gate electrode, or may be formed to be larger (in width) than the gate electrode.

[0043]

The gate electrode or electrode is formed on the gate insulation film normally in a shape for use in a semiconductor device or a shape that has a concave portion in a lower end portion. Herein, the "single gate electrode" is defined as a gate electrode consisting of a monolayer or multilayer conductive film and formed into a single inseparable piece. The gate electrode may have a

side wall insulation film on each side surface. The gate electrode is normally not specifically limited so long as it is used for a semiconductor device, and there can be enumerated conductive films of: polysilicon; metals including copper and aluminum; high-melting metals including tungsten, titanium, and tantalum; and silicides of high-melting metals, in the form of a single-layer or a multi-layer. The gate electrode should properly be formed with a film thickness of, for example, about 50 to 400 nm. It is to be noted that a channel region is formed under the gate electrode.

[0044]

The memory function body includes a film or region that has a function to retain charges, store and retain charges, trap charges or retain a charge polarized state. Materials implementing these functions include: silicon nitride; silicon; silicate glass including impurities such as phosphorus or boron; silicon carbide; alumina; high-dielectric substances such as hafnium oxide, zirconium oxide, or tantalum oxide; zinc oxide; and metals. The memory function body may be formed into single-layer or multi-layer structure of: for example, an insulating film containing a silicon nitride film; an insulating film incorporating a conductive film or a semiconductor layer inside; and an insulating film containing one or more

conductor dots or semiconductor dots. Among these, the silicon nitride is preferable because it can achieve a large hysteresis property by the presence of a number of levels for trapping electric charges, and has good holding characteristics in that the electric-charge holding time is long and that there hardly occurs leakage of electric charges caused by generation of leakage paths, and further because it is a material normally used in LSI process.

[0045]

Use of an insulating film containing inside an insulating film having a charge holding function such as a silicon nitride film enables increase of reliability relating to memory holding. Since the silicon nitride film is an insulator, electric charges of the entire silicon nitride film will not be immediately lost even if part of the electric charges are leaked. Further, in the case of arraying a plurality of memory elements, even if the distance between the memory elements is shortened and adjacent memory function bodies come into contact with each other, information stored in each memory function body is not lost unlike the case where the memory function body is made from a conductor. Also, it becomes possible to dispose a contact plug closer to the memory function body, or in some cases it becomes possible to dispose the contact plug so as to overlap with the memory function body, which

facilitates miniaturization of the memory elements.

[0046]

For further increase of the reliability relating to the memory holding, the insulation film having a function of holding electric charges is not necessarily needed to be in the film shape, and insulators having the function of holding an electric charge may preferably be present in an insulating film in a discrete manner. More specifically, such insulating films may be dispersed like dots within a material having difficulty in holding electric charges, such as silicon oxide.

[0047]

Also, use of an insulating film containing inside a conductive film or a semiconductor layer as a charge holding portion enables free control of the quantity of electric charges injected into the conductor or the semiconductor, thereby bringing about an effect of facilitating achieving a multi-valued memory cell.

[0048]

Further, using an insulator film containing one or more conductor or semiconductor dots as a memory function body facilitates execution of write and erase by direct tunneling of electric charges, thereby bringing about an effect of reduced power consumption.

[0049]

Moreover, it is acceptable to use, as a memory function body, a ferroelectric film such as PZT and PLZT whose polarization direction is changed by an electric field. In this case, electric charges are substantially generated by polarization on the surface of the ferroelectric film and retained in the state. Therefore, electric charges are supplied from outside the film that has the memory function, and a hysteresis characteristic similar to that of the film that traps electric charges can be obtained. In addition, since there is no need to inject electric charges from outside the film and the hysteresis characteristic can be obtained only by the polarization of the electric charges in the film, high-speed write and erase is achievable.

[0050]

It is preferable that the memory function body further contains a region that obstructs escape of electric charges or a film having a function of obstructing escape of electric charges. Materials fulfilling the function of obstructing escape of electric charges include a silicon oxide.

[0051]

Preferably, the charge retention film contained in the memory function body is formed on both sides of the gate electrode directly or through an insulating film, and

it is disposed on the semiconductor substrate (a well region, a body region, or a source/drain region or a diffusion layer region) through the gate insulating film or the insulating film. The charge retention films on both sides of the gate electrode are preferably formed so as to cover all or part of side surfaces of the gate electrode directly or through the insulating film. In an application where the gate electrode has a recess portion on the lower edge side, the charge retention film may be formed so as to fill the entire recess portion or part of the recess portion directly or through the insulating film.

[0052]

Preferably, the gate electrode is formed only on the side surface of the memory function body, or the upper portion of the charge holding portion is not covered with the gate electrode. In such arrangement, it becomes possible to dispose a contact plug closer to the gate electrode, which facilitates miniaturization of the memory elements. Also, the memory elements having such simple disposition are easily manufactured, resulting in an increased yield.

[0053]

If a conductive film is used as a charge retaining film, it is preferable to place such a film via an insulation film such that the charge retaining film does

not touch the semiconductor substrate (well region, body region, source/drain region, or diffusion region) or the gate electrode. For example, there may be a stacked structure of a conductive film and an insulation film, a structure in which dots of a conductive film are scattered in an insulation film, a structure in which the conductive or semiconductor charge retention film is included in a side wall insulation film on a side surface of the gate, etc.

[0054]

The source/drain regions, which have a conductivity type opposite to that of the semiconductor substrate or the well region, are respectively disposed on opposite sides of the gate electrode of the charge retention films. A junction of the source/drain region and the semiconductor substrate or the well region should preferably have a steep slope of impurity concentration. The reason for the above is that hot electrons and hot holes are efficiently generated at a low voltage, and high-speed operation can be achieved at a lower voltage. The junction depth of the source/drain region is not specifically limited and is allowed to be properly adjusted according to the performance and so on of the semiconductor storage device desired to be obtained. When a SOI substrate is employed as a semiconductor substrate, the

source/drain region may have a junction depth smaller than the film thickness of the surface semiconductor layer. However, the source/drain region should preferably have a junction depth almost equal to the film thickness of the surface semiconductor layer.

[0055]

The source/drain region may be arranged so as to overlap with the gate electrode end or arranged so as to meet the gate electrode end or arranged so as to be offset with respect to the gate electrode end. In particular, in the case of offset, the easiness of inversion of the offset region under the charge retaining film is largely changed by the quantity of charges accumulated in the memory function body when the voltage is applied to the gate electrode, increasing the memory effect and reducing the short-channel effect. Therefore, this arrangement is preferable. However, since a drive current between the source/drain regions is significantly reduced if the offset is excessive, it is preferred that the amount of offset, i.e., a distance from one gate electrode end to the nearer source/drain region in the direction of the gate length should preferably be shorter than the thickness of the charge retaining film in the direction parallel to the gate length direction. What is particularly important is that at least part of the region having the charge retention

function in the memory function body overlaps with part of the source/drain region that is the diffusion region. The reason for the above is that the essence of the memory elements that constitute the semiconductor storage device of the present invention is to rewrite the storage by the electric field intersecting the memory function body due to a voltage difference between the gate electrode and the source/drain region existing only in the side wall portion of the memory function body.

[0056]

The source/drain region may be partially extended to a position higher than the surface of the channel region, i.e., the lower surface of the gate insulation film. In this case, it is proper that a conductive film integrated with this source/drain region is constructed while being laminated on the diffusion region formed in the semiconductor substrate. As the conductive film, there can be enumerated, for example, semiconductor of polysilicon, amorphous silicon or the like, silicide, aforementioned metals, high-melting-point metals and so on. Among others, polysilicon is preferable. The reason for the above is that the polysilicon, of which the impurity diffusion speed is significantly greater than that of the semiconductor layer, easily tolerates a shallowed junction depth of the source/drain region in the semiconductor layer

and easily suppresses the short-channel effect. In this case, it is preferable to provide an arrangement that part of this source/drain region and the gate electrode hold at least part of the memory function body therebetween.

[0057]

The memory element of the present invention can be formed by the ordinary semiconductor process according to a method similar to the method of forming a side wall spacer of a single layer or laminate structure on the side wall of the gate electrode or word line. In concrete, there can be enumerated: a method comprising forming a gate electrode or a word line, thereafter forming a single layer film or multilayer film including a charge retaining film, such as a charge retaining film, a charge retaining film/insulation film, an insulation film/charge retaining film, and an insulation film/charge retaining film/insulation film, and leaving the film or films in a side wall spacer shape by etching back under appropriate conditions; a method comprising forming an insulation film or a charge retaining film, leaving the film in a side wall spacer shape by etching back under appropriate conditions, further forming a charge retaining film or insulation film and leaving the film in a side wall spacer shape by etching back under appropriate conditions; a method comprising coating or depositing, on a semiconductor substrate

including a gate electrode, an insulation film material in which a particulate charge retaining material is distributed, and leaving the insulation film material in a side wall spacer shape by etching back under appropriate conditions; a method comprising forming a gate electrode, thereafter forming the single layer film or the multilayer film and carrying out patterning by using a mask, and so on. Moreover, there can be enumerated a method comprising forming a charge retaining film, a charge retaining film/insulation film, an insulation film/charge retaining film, or an insulation film/charge retaining film/insulation film before forming a gate electrode or an electrode, forming an opening through the film or films in a region that becomes a channel region, forming a gate electrode material film on the entire upper surface of the semiconductor substrate and patterning this gate electrode material film in a shape, which is larger than the opening in size and encompasses the opening.

[0058]

When a memory cell array is constructed by arranging the memory elements of the present invention, the best mode of the memory elements is to satisfy, for example, all the required conditions:

(1) The function of a word line is possessed by the integrated body of the gate electrodes of a plurality

of memory elements;

(2) Formed on opposite sides of the word line is a memory function body that continuously extends along the word line;

(3) A material that retains electric charges in the memory function body is an insulator, and in particular, a silicon nitride film;

(4) The memory function bodies are constructed of an ONO (Oxide Nitride Oxide) film, and the silicon nitride film has a surface roughly parallel to the surface of the gate insulation film;

(5) The silicon nitride film in each memory function body is separated from the word line and the channel region by the silicon oxide film;

(6) A region having a function of retaining charges (e.g., a region formed of silicon nitride film) in each memory function body overlaps with the corresponding diffusion region;

(7) The thickness of the insulation film, which separates the silicon nitride film that has a surface roughly parallel to the surface of the gate insulation film from the channel region or the semiconductor layer differs from the thickness of the gate insulation film;

(8) Write and erase operations of one memory element are executed by a single word line;

(9) There is no electrode (word line), on each memory function body, which has a function to assist the write and erase operations; and

(10) A portion put in contact with the diffusion region right under each memory function body has a region where the impurity concentration of the conductivity type opposite to the conductivity type of the diffusion region is high.

The memory elements are not required to satisfy all of these requirements.

[0059]

When some of the above requirements are satisfied, there are most preferable combinations of requirements. For example, a most preferable combination resides in that (3) a material that retains electric charges in the memory function body is an insulator, and in particular, a silicon nitride film; (9) there is no electrode (word line), on each memory function body, which has a function to assist the write and erase operations; and (6) a region having a function of retaining charges (e.g., a region formed of silicon nitride film) in each memory function body overlaps with the corresponding diffusion region. When the material that retains electric charges in the memory function body consists of an insulator, and there is no electrode (word line), on each

memory function body, which has a function to assist the write and erase operations, it has been found out that the write operation is preferably executed only in the case where the insulating film (silicon nitride film) and the diffusion layer overlap with each other. That is, when the requirements (3) and (9) are satisfied, satisfying the requirement (6) has been found to be essential. On the other hand, when the charge retaining region in the memory function body consists of a conductor, the write operation was able to be executed even when the conductor in the memory function body and the diffusion region do not overlap with each other (because the conductor in the memory function body assists the write operation by capacitive coupling with the write electrode). Moreover, when there is an electrode that has the function to assist the write and erase operations on the memory function body, the write operation was able to be executed even when the insulating film in the memory function body and the diffusion region do not overlap with each other.

[0060]

However, when an insulator instead of a conductor retains electric charges in the memory function body, and there is no electrode on the memory function body on the gate electrode, the following great advantages are obtained.

[0061]

First, a bit line contact can be arranged closer to the memory function body located on the word line side wall, or even if the memory elements are put close to each other in distance, the plurality of memory function bodies do not interfere with one another, and the storage information can be retained. Therefore, the miniaturization of the memory elements is facilitated. When the charge retaining region in the memory function body consists of a conductor, interference occurs between the adjacent charge retaining regions by capacitive coupling as the distance between the memory elements is reduced, and the storage information cannot be retained.

[0062]

Moreover, when the charge retaining region in the memory function body consists of an insulator (e.g., silicon nitride film), there is no need to make the memory function bodies of one memory cell independent of those of another memory cell. For example, the memory function bodies continuously formed on both sides of and along one word line shared by a plurality of memory cells are not required to be isolated every memory cell, and it is possible to share the memory function bodies formed on both sides of one word line by a plurality of memory cells that share the word line. Therefore, the photolithography and

etching process for isolating the memory function bodies become unnecessary, and the manufacturing process is simplified. Furthermore, the alignment margin for the photolithography process and the film etching margin become unnecessary. Therefore, the margin between the memory cells can be reduced. Therefore, in comparison with the case where the charge retaining region in the memory function body consists of a conductor (e.g., polycrystalline silicon film), the memory cell occupation area can be miniaturized even if the same microfabrication level is applied. (The case where the charge retaining region in the memory function body consists of a conductor would need the photolithography and etching process for separating the memory function bodies every memory cell, the photolithography alignment margin and the film etching margin.)

[0063]

Furthermore, since the element structure is simple in that no electrode having the function to assist the write and erase operations is located on the memory function bodies, the number of fabrication process steps is reduced, and the yield can be improved. Therefore, combination with the transistors that constitute a logic circuit and an analog circuit can be facilitated.

[0064]

Furthermore, we have found that as a very important design matter, even if the material that retains electric charges in the memory function body consists of an insulator, and there is no electrode (word line), on each memory function body (by satisfying the two requirements, the very important effects of the reduction of cell occupation area and the improvement in the yield by simplification of the fabrication process are obtained), the charge retaining region in the memory function body is overlapped with the corresponding diffusion layer, whereby the write and erase operations can be executed at a very low voltage. In concrete, we have ascertained that the write and erase operations can be executed at a low voltage of not higher than 5 V. This operation produces a very large effect in terms of circuit design. There is no need to make a high voltage in a chip dissimilarly from the flash memory, and therefore, a charge pump circuit, which requires an enormous occupation area, can be eliminated or reduced in scale. Particularly, when a small-scale capacity memory for adjustment is built in a logic LSI, the occupation area of the memory section is dominated by the occupation area of the peripheral circuit for driving the memory cells than the memory cells. Therefore, it is most effective to eliminate or reduce the scale of the memory cell voltage booster circuit in order to reduce the chip

size.

[0065]

This is why satisfying the requirements (3), (9) and (6) is particularly preferable.

[0066]

In an memory cell array wherein a plurality of memory elements are arrayed, it is preferred that the memory elements that are arranged sharing a single word line, each memory element comprising: the single word line formed on a semiconductor layer via a gate insulation film; a channel region arranged under the single word line; diffusion regions arranged on opposite sides of the channel region; memory function bodies formed only on both sides of the word line and having a function to retain electric charges, each of the memory function bodies existing over part of the channel region and the corresponding part of each of the diffusion regions, straddling a boundary therebetween, wherein the memory function body is formed of an insulation material, and the plurality of memory elements sharing the one word line share the memory function bodies formed on the opposite sides of the word line. The above arrangement substantially satisfies the requirements (3), (9) and (6). Thus, even in the memory cell array having the memory elements arrayed, the aforementioned effects and advantages are obtained. Further, because only a single

word line is selected in rewriting the memory elements on the sides of the single word line, the number of word lines required for the memory operation becomes minimum, so that the memory cell array is integrated at a higher packing density.

[0067]

The semiconductor storage device of the present invention in which a logic element, a logic circuit or the like are combined can be used for the portable electronic equipment, in particular for portable information terminals. The portable electronic equipment includes portable information terminals, portable telephones, game machines and the like.

[0068]

The memory element will be described in more detail in the following embodiments.

[0069]

(First Embodiment)

Fig. 1 shows a sectional view of one example of the memory element. The memory element 1 is formed on a P-type well region 102 formed on the surface of a semiconductor substrate 101. A gate electrode 104 is formed on the P-type well region 102 via a gate insulation film 103. On both sides of the gate electrode 104, memory function portions 105a and 105b are formed. The memory

function portions herein indicate, of memory function bodies or charge retaining films, those where electric charges are actually retained by the rewrite operation. In an example shown in Fig. 1, a silicon nitride film 109, which has a trap level for retaining electric charges and serves as a charge retaining film, covers the upper surface and the side surfaces of the gate electrode 104, and the portions of the silicon nitride film 109 located on both side walls serve as the memory function portions 105a, 105b. Diffusion regions 107a and 107b function as a source region and a drain region, respectively. The diffusion regions 107a and 107b have an offset structure. That is, the diffusion regions 107a and 107b do not reach the region 121 located under the gate electrode, and the offset regions 120 under the charge retaining film (silicon nitride film 109) constitute part of the channel region.

[0070]

Fig. 2 shows another example of the memory element. The difference between a memory element 2 and the memory element 1 of Fig. 1 is that memory function bodies 131a, 131b respectively have a trap level for retaining electric charges, with the structure in which a silicon nitride film 131 as a charge retaining film is held between silicon oxide films 111 and 112. As shown in Fig. 2, with the structure in which the silicon nitride film is held

between the silicon oxide films, charge injection efficiency during the rewrite operation is increased, and higher-speed operation becomes possible.

[0071]

In Fig. 2, the silicon nitride film 242 may be replaced by a ferroelectric substance. Further, in Fig. 1, the memory function bodies 105a and 105b may have a structure in which particles constructed of a conductor or a semiconductor of a nanometer size are distributed in scattered dots in an insulation film 111 (see Fig. 2B). In this case, it is difficult for an electric charge to tunnel its way through the dots since the quantum effect is excessive when the particle has a size smaller than 1 nm, and no remarkable quantum effect appears at the room temperature when the size exceeds 10 nm. Therefore, the diameter of the particle should preferably be within a range of 1 nm to 10 nm. Furthermore, the memory function bodies 131a, 131b are not necessarily required to have a side wall spacer shape different from the memory element 2 (Fig. 2). For example, in the memory element 1 (Fig. 1), although the silicon nitride film 109 having a trap level for retaining electric charges is arranged on the upper surface and the side surfaces of the gate electrode 104, the memory function portions that substantially retain electric charges are both sides wall portions (105a, 105b)

of the gate electrode 104. That is, the silicon nitride film 109 is only required to be formed in these regions.

[0072]

The principle of write operation of the memory element will be described with reference to Fig. 3 and Fig. 4. In this case, the description is based on the case where the entire bodies of the memory function bodies 131a and 131b have a function to retain electric charges.

[0073]

The term of "write" herein means the injection of electrons into the memory function bodies 131a and 131b when the memory element 1, 2 is the N-channel type. Hereinafter, the description is provided on the assumption that the memory element 1, 2 is the N-channel type.

[0074]

In order to inject an electron (execute write) into the second memory function body 131b, as shown in Fig. 3, a first diffusion region 107a (having an N-type conductivity) and second diffusion region 107b (having an N-type conductivity) are made to serve as a source electrode and a drain electrode, respectively. For example, a voltage of 0 V is applied to the first diffusion region 107a and the P-type well region 102, a voltage of +5 V is applied to the second diffusion region 107b, and a voltage of +5 V is applied to the gate electrode 104. According to

the above-mentioned voltage conditions, an inversion layer 226 extends from the first diffusion region 107a (source electrode), but it does not reach the second diffusion region 107b (drain electrode), generating a pinch-off point. An electron is accelerated from the pinch-off point to the second diffusion region 107b (drain electrode) by a high electrical field and becomes a so-called hot electron (high energy conduction electron). Write is executed by the injection of this hot electron into the second memory function body 131b. Since no hot electron is generated in the vicinity of the first memory function body 131a, write is not executed.

[0075]

In this manner, an electron is injected into the second memory function body 131b so that the write can be executed.

[0076]

On the other hand, in order to inject an electron (execute write) into the first memory function body 131a, as shown in Fig. 4, the second diffusion region 107b and the first diffusion region 107a are made to serve as the source electrode and the drain electrode, respectively. For example, a voltage of 0 V is applied to the second diffusion region 107b and the P-type well region 102, a voltage of +5 V is applied to the first diffusion

region 107a, and a voltage of +5 V is applied to the gate electrode 104. As described above, by exchanging the source and drain regions reversely to the case where an electron is injected into the second memory function body 131b, write can be executed by injecting an electron into the first memory function body 131a.

[0077]

Next, the principle of erase operation of the memory element will be described with reference to Fig. 5 and Fig. 6.

[0078]

According to a first method for erasing the information stored in the first memory function body 131a, as shown in Fig. 5, a positive voltage (e.g., +5 V) is applied to the first diffusion region 107a, a voltage of 0 V is applied to the P-type well region 102, a reverse bias is applied to a PN junction of the first diffusion region 107a and the P-type well region 102, and a negative voltage (e.g., -5 V) is further applied to the gate electrode 104. At this time, the potential slope becomes steep, in particular, in the vicinity of the gate electrode 104 at the PN junction due to the influence of the gate electrode to which the negative voltage is applied. Accordingly, a hot hole (high energy hole) is generated on the P-type well region 102 side of the PN junction due to band-to-band

tunneling. This hot hole is drawn toward the gate electrode 104 that has a negative potential, and consequently, the hole is injected into the first memory function body 131a. As described above, the erase of the first memory function body 131a is executed. In this case, it is proper to apply a voltage of 0 V to the second diffusion region 107b.

[0079]

When erasing the information stored in the second memory function body 131b, it is proper to exchange the potential of the first diffusion region with the potential of the second diffusion region in the aforementioned case.

[0080]

According to a second method for erasing the information stored in the first memory function body 131a, as shown in Fig. 6, a positive voltage (e.g., +4 V) is applied to the first diffusion region 107a, a voltage of 0 V is applied to the second diffusion region 107b, a negative voltage (e.g., -4 V) is applied to the gate electrode 104, and a positive voltage (e.g., +0.8 V) is applied to the P-type well region 102. In this case, a forward voltage is applied across the P-type well region 102 and the second diffusion region 107b, injecting an electron into the P-type well region 102. The injected

electron diffuses to a PN junction of the P-type well region 102 and the first diffusion region 107a and become hot electrons by being accelerated there by an intense electric field. This hot electron generates an electron-hole pair at the PN junction. That is, by applying the forward voltage across the P-type well region 102 and the second diffusion region 107b, the electron injected into the P-type well region 102 becomes a trigger to generate a hot hole at the PN junction located on the opposite side. The hot hole generated at the PN junction is drawn toward the gate electrode 104 that has a negative potential, and consequently, the hole is injected into the first memory function body 131a.

[0081]

According to the second method, even when only a voltage insufficient for the generation of a hot hole by band-to-band tunneling is applied to the PN junction of the P-type well region and the first diffusion region 107a, the electron injected from the second diffusion region 107b becomes a trigger to generate an electron-hole pair at the PN junction, allowing a hot hole to be generated. Therefore, the voltage during the erase operation can be lowered. Particularly, when an offset region 120 (see Figs. 1 and 2) exists, the effect that the PN junction becomes steep due to the gate electrode to which the negative

potential is applied is a little, and therefore, it is difficult to generate a hot hole by band-to-band tunneling. The second method makes up for the defect, and the erase operation can be achieved at a low voltage.

[0082]

In erasing the information stored in the first memory function body 131a, a voltage of +5 V must be applied to the first diffusion region 107a according to the first erase method, whereas a voltage of +4 V is sufficient according to the second erase method. As described above, according to the second method, the voltage during erase can be reduced. Therefore, power consumption is reduced, and the deterioration of the memory element due to the hot carrier can be restrained.

[0083]

Moreover, by either one of the erase methods, overerase does not easily occur in the memory element. The term of "overerase" here is a phenomenon that the threshold value is lowered without saturation as the amount of holes accumulated in the memory function body increases. This is a serious problem in EEPROM (Electrically Erasable Programmable Read-Only Memory) represented by a flash memory, and there occurs a fatal malfunction that memory cell selection becomes impossible particularly when the threshold value becomes negative. On the other hand, in

the memory element of the semiconductor storage device of the present invention, only electrons are induced under the memory function bodies even when a large amount of holes are accumulated in the memory function body, and almost no influence is exerted on the potential of the channel region under the gate insulation film. The threshold value during erase is determined by the potential under the gate insulation film, and therefore, overerase does not easily occur.

[0084]

The principle of read operation of the memory element will be further described with reference to Fig. 7.

[0085]

In reading the information stored in the first memory function body 131a, as shown in Fig. 7, the transistor is operated by making the first diffusion region 107a and the second diffusion region 107b serve as a source electrode and a drain electrode, respectively. For example, a voltage of 0 V is applied to the first diffusion region 107a and the P-type well region 102, a voltage of +1.8 V is applied to the second diffusion region 107b, and a voltage of +2 V is applied to the gate electrode 104. In this case, when no electron is accumulated in the first memory function body 131a, a drain current easily flows. When electrons are accumulated in the first memory function body

131a, the inversion layer is not easily formed in the vicinity of the first memory function body 131a, and therefore, a drain current hardly flows. Therefore, by detecting the drain current, the storage information of the first memory function body 131a can be read. In particular, when read is executed by giving a voltage that causes the pinch-off operation, the state of charges accumulated in the first memory function body 131a can be more accurately determined without being influenced by the presence or absence of charges in the memory function body 131b. At this time, the presence or absence of charge accumulation in the second memory function body 131b does not affect the drain current because a pinch-off point is generated in the vicinity of the drain.

[0086]

In reading the information stored in the second memory function body 131b, the transistor is operated by making the second diffusion region 107b and the first diffusion region 107a serve as the source electrode and the drain electrode, respectively. Although not shown, it is proper to apply, for example, a voltage of 0 V to the second diffusion region 107b and the P-type well region 102, apply a voltage of +1.8 V to the first diffusion region 107a and apply a voltage of +2 V to the gate electrode 104. As described above, by exchanging the source and drain

regions reversely to the case where the information stored in the first memory function body 131a is read, the information stored in the second memory function body 131b can be read.

[0087]

If the channel region (offset regions 120) that is not covered with the gate electrode 104 is left, then the inversion layer is lost or formed depending on the presence or absence of surplus electric charges of the memory function bodies 131a and 131b in the channel region that is not covered with the gate electrode 104, and consequently, a great hysteresis (a change in the threshold value) is obtained. It is to be noted that the drain current is largely reduced when the width of the offset region 120 is excessively large, and the read speed is significantly slowed. Therefore, it is preferable to determine the width of the offset region 120 so that sufficient hysteresis and read speed can be obtained.

[0088]

Even when the diffusion regions 107a and 107b reached the ends of the gate electrode 104, i.e., even when the diffusion regions 107a and 107b and the gate electrode 104 overlap with each other, the threshold value of the transistor was scarcely changed by the write operation. However, a parasitic resistance at the ends of the source

and drain was largely changed, and the drain current was largely reduced (by an order of magnitude or more). Therefore, read can be executed by detecting the drain current, and a function as a memory can be obtained. However, when a larger memory hysteresis effect is needed, it is preferred that the diffusion regions 107a and 107b do not overlap with the gate electrode 104 (the offset region 120 exists).

[0089]

By the aforementioned operation method, 2-bit write and erase per transistor can be selectively achieved. Moreover, by arranging memory elements with a word line WL connected to the gate electrodes 104 of the memory elements and with a first bit line BL1 and a second bit line BL2 connected to the first diffusion regions 107a and the second diffusion regions 107b, respectively, a memory cell array can be constructed.

[0090]

Moreover, according to the aforementioned operation method, the 2-bit write and erase per transistor are executed by exchanging the source electrode with the drain electrode. However, the device may be operated as a 1-bit memory by fixing the source electrode and the drain electrode. In this case, it is possible to make one of the source and drain regions have a common fixed voltage, and

the number of bit lines connected to the source and drain regions can be reduced by half.

[0091]

As is apparent from the above description, in the memory element of the semiconductor storage device of the present invention, the memory function bodies are formed independently of the gate insulation film and formed on both sides of the gate electrode, and therefore, the 2-bit operation can be achieved. Moreover, the memory function bodies are separated by the gate electrode, and therefore, interference during rewrite is effectively restrained. Furthermore, the gate insulation film, which is separated from the memory function body, can therefore restrain the short-channel effect by being reduced in film thickness. Therefore, the miniaturization of the memory element and also the semiconductor storage device is facilitated.

[0092]

(Second Embodiment)

The memory element of the present embodiment is constructed of memory function bodies 261 and 262, which are constructed of a region for retaining electric charges (this may be a region for storing electric charges, or a film having the function to retain electric charges) and a region for restraining the escape of electric charges (this

may be a film that has a function to restrain the escape of electric charges). For example, as shown in Fig. 8, the memory function bodies have an ONO structure. That is, the memory function bodies 261, 262 are each constructed of a silicon nitride film 242 that is held between silicon oxide films 241 and 243. The silicon nitride film 242 herein functions to retain electric charges. Further, the silicon oxide films 241, 243 function as films for restraining the escape of electric charges.

[0093]

Also, the region (silicon nitride film 242) for holding or retaining electric charges in the memory function bodies 261, 262 are overlapped with the diffusion layer regions 212, 213. Herein, the term "overlap" is used to refer to the state that at least part of the region (silicon nitride film 242) for retaining electric charges is present on at least part of the diffusion layer regions 212, 213. It is noted that there are shown a semiconductor substrate 211, a gate insulating film 214, and an offset region 271 (between the gate electrode 217 and the diffusion layer regions 212, 213). Though unshown in the drawing, the uppermost surface of the semiconductor substrate 211 under the gate insulating film 214 is a channel region.

[0094]

An effect produced by the arrangement that the silicon nitride film 242 serving as the region for retaining electric charges in the memory function bodies 261 and 262 overlap with the diffusion regions 212 and 213 will be described.

[0095]

Fig. 9 is an enlarged view of peripheral portions of the right side memory function body 262. As shown in Fig. 9, W1 shows the amount of offset of a gate electrode 214 with respect to a diffusion region 213. Further, W2 shows the width of the memory function body 262 in a cross-sectional plane in the channel-length direction of the gate electrode 217. Since the end of the silicon nitride film 242 remote from the gate electrode 217 is coincides with the end of the memory function body 262 remote from the gate electrode 217 at the memory function body 262, the width of the memory function body 262 was defined as W2. W2 - W1 is the amount of overlap of the memory function body 262 with the diffusion region 213. The amount of overlap of the memory function body 262 with the diffusion region 213 is expressed by W2 - W1. What is important here is that the memory function body 262 constructed of the silicon nitride film 242 of the memory function body 262 overlaps with the diffusion region 213, i.e., the arrangement that the relation: W2 > W1 is

satisfied.

[0096]

In the case where an edge of a silicon nitride film 242a on the side away from the gate electrode in a memory function body 262a is not aligned with an edge of the memory function body 262a on the side away from the gate electrode as shown in Fig. 10, W2 may be defined as the width from the edge of the gate electrode to the edge of the silicon nitride film 242a on the side away from the gate electrode.

[0097]

Fig. 11 shows a drain current Id in the structure of Fig. 9 with the width W2 of the memory function body 262 being fixed to 100nm and the offset amount W1 being varied. Herein, the drain current is obtained by device simulation performed under the conditions that the memory function body 262 is in erase state (positive holes are stored), and the diffusion layer regions 212, 213 are set to be a source electrode and a drain electrode, respectively.

[0098]

As shown in Fig. 11, with W1 being 100nm or more (i.e., when the silicon nitride film 242 and the diffusion layer region 213 are not overlapped), the drain current shows rapid reduction. Since a drain current value

is almost in proportion to a read operation speed, memory performance is rapidly deteriorated when W1 is 100nm or more. In the range where the silicon nitride film 242 and the diffusion layer region 213 are overlapped, the drain current shows mild reduction. Therefore, taking a manufacturing dispersion into consideration, it is difficult to obtain a memory function unless at least part of the silicon nitride film 242 that is a film having a function of holing electric charges is overlapped with the source/drain region.

[0099]

Based on the above-described result of the device simulation, a memory cell array is manufactured with W2 being fixed to 100nm, and W1 being set to 60nm and 100nm as design values. When W1 is 60nm, the silicon nitride film 242 is overlapped with the diffusion layer regions 212, 213 by 40nm as a design value, and when W1 is 100nm, there is no overlap as a design value. As a result of measuring read time of these memory cell arrays in comparison with the worst cases in consideration to dispersion, it was found out that the case where W1 was 60nm as a design value was 100 times faster in readout access time. From a practical standpoint, it is preferable that the read access time is 100 nanoseconds or less per bit. It was found out, however, that this condition was never satisfied in the

case of W1=W2. It was also found out that W2-W1>10nm was more preferable in consideration to manufacturing dispersion.

[0100]

It is preferable for reading information stored in the memory function body 261 (region 281) to set the diffusion layer region 212 as a source electrode and the diffusion layer region 213 as a drain region similar to the embodiment 1 and to form a pinchoff point on the side closer to the drain region in the channel region. More specifically, in reading information stored in either one of two memory function bodies, the pinch-off point is preferably formed in a region closer to the other memory function body in the channel region. This makes it possible to detect memory information in the memory function body 261 with good sensitivity regardless of the storage condition of the memory function body 262, resulting in large contribution to implementation of two-bit operation.

[0101]

In the case of storing information only in one side out of the two memory function bodies, or in the case of using these two memory function bodies in the same storing condition, a pinch-off point is not necessarily formed in read operation.

[0102]

Although not shown in Fig. 8, a well region (P type well in the case of N-channel device) is preferably formed on the surface of the semiconductor substrate 211. Forming the well region facilitates control of other electric characteristics (withstand voltage, junction capacitance, and short channel effect) while maintaining impurity concentration of the channel region optimum for memory operation (rewrite operation and read operation).

[0103]

From the point of view of improving the retention characteristic of the memory, the memory function body should preferably include a charge retaining film having the function to retain electric charges and an insulation film. This embodiment employs a silicon nitride film 242 that has a level for trapping electric charges as a charge retaining film and silicon oxide films 241 and 243 that have the operation of preventing the dissipation of electric charges accumulated in the charge retaining film as an insulation film. By the memory function body that includes the charge retaining film and the insulation film, the retention characteristic can be improved by preventing the dissipation of electric charges. Moreover, the volume of the charge retaining film can be moderately reduced in comparison with the case where the memory function body is

constructed only of the charge retaining film. By the moderate reduction of the volume of the charge retaining film, the movement of electric charges in the charge retaining film is limited, thus making it possible to restrain the occurrence of a characteristic change due to the movement of electric charges during the retention of the storage.

[0104]

Also, it is preferable that the memory function body contains a charge retaining film disposed approximately parallel to the surface of the gate insulating film. In other words, it is preferable that the surface of the charge retaining film in the memory function body is disposed so as to have a constant distance from the surface of the gate insulating film. More particularly, as shown in Fig. 12, a charge retaining film 242a in the memory function body 262 has a face approximately parallel to the surface of the gate insulating film 214. In other words, the charge retaining film 242a is preferably formed to have a uniform height from the height corresponding to the surface of the gate insulating film 214. The presence of the charge retaining film 242a approximately parallel to the surface of the gate insulating film 214 in the memory function body 262 makes it possible to effectively control easiness of formation of an inversion layer in the offset

region 271 with use of an amount of electric charges stored in the charge retaining film 242a, thereby enabling increase of memory effect. Also, by placing the charge retaining film 242a approximately parallel to the surface of the gate insulating film 214, change of memory effect may be kept relatively small even with a dispersed offset amount (W1), enabling restraint of memory effect dispersion. In addition, movement of electric charges toward upper side of the charge retaining film 242a may be suppressed, and therefore characteristic change due to the movement of electric charges during memory holding may be restrained.

[0105]

Furthermore, the memory function body 262 preferably contains an insulating film (e.g., a portion of the silicon oxide film 244 on the offset region 271) that separates the charge retaining film 242a approximately parallel to the surface of the gate insulating film 214 from the channel region (or the well region). This insulating film may restrain dissipation of the electric charges stored in the charge retention film, thereby contributing to obtaining a memory device with better holding characteristics.

[0106]

It is noted that controlling the film thickness of the charge retaining film 242a as well as controlling

the film thickness of the insulating film under the charge retaining film 242a (a portion of the silicon oxide film 244 on the offset region 271) to be constant make it possible to keep the distance from the surface of the semiconductor substrate to the electric charges stored in the charge retention film approximately constant. More particularly, the distance from the surface of the semiconductor substrate to the electric charges stored in the charge retention film may be controlled to be within the range from a minimum film thickness value of the insulating film under the charge retaining film 242a to the sum of a maximum film thickness of the insulating film under the charge retaining film 242a and a maximum film thickness of the charge retaining film 242a. Consequently, the concentration of electric line of force generated by the electric charges stored in the retaining film 242a may be roughly controlled, and therefore dispersion of the degree of memory effect of the memory device may be minimized.

[0107]

(Third Embodiment)

In this embodiment, as shown in Fig. 13, a charge retention film 242 of a memory function body 262 has an approximately uniform film thickness. The charge retention film 242 is configured to be disposed

approximately parallel to the surface of the gate insulating film 214 (arrow 281) and disposed extending in direction approximately parallel to the side face of the gate electrode 217 (arrow 282).

[0108]

When a positive voltage is applied to the gate electrode 217, electric line of force in the memory function body 262 passes the silicon nitride film 242 total two times through the first portion 281 and the second portion 282 as shown with an arrow 283. It is noted that when a negative voltage is applied to the gate electrode 217, the direction of electric line of force is reversed. Herein, a dielectric constant of the silicon nitride film 242 is approx. 6, while a dielectric constant of silicon oxide films 241, 243 is approx. 4. Eventually, an effective dielectric constant of the memory function body 262 in the direction of electric line of force (arrow 283) becomes larger than that in the case where the charge retention film includes only the first portion 281, which makes it possible to decrease potential difference between the both edges of the electric line of force. More specifically, much part of the voltage applied to the gate electrode 217 is used to reinforce electric fields in the offset region 271.

[0109]

Electric charges are injected into the silicon nitride film 242 in rewrite operation because generated electric charges are pulled by electric fields in the offset region 271. As a consequence, the silicon nitride film 242 including the second portion 282 increases the electric charges injected into the memory function body 262 in rewrite operation, thereby increasing a rewrite speed.

[0110]

In the case where the portion of the silicon oxide film 243 is a silicon nitride film, more specifically, in the case where the charge retention film is not flat against the height corresponding to the surface of the gate insulating film 214, movement of electric charges toward upper side of the silicon nitride film becomes outstanding, and holding characteristics are deteriorated.

[0111]

Instead of silicon nitride film, the charge retention film is more preferably formed from high-dielectric substances such as hafnium oxide having extremely large dielectric constant.

[0112]

Further, the memory function body more preferably includes an insulating film (a portion of the 241 on the silicon oxide film on the offset region 271) that separates the charge retention film approximately

parallel to the surface of the gate insulating film from the channel region (or the well region). This insulating film may restrain dissipation of the electric charges stored in the charge retention film, thereby enabling further improvement of holding characteristics.

[0113]

Also, the memory function body more preferably includes an insulating film (a portion of the silicon oxide film 241 in contact with the gate electrode 217) that separates the gate electrode from the charge retention film extending in the direction approximately parallel to the side face of the gate electrode. This insulating film may prevent injection of electric charges from the gate electrode into the charge retention film and prevent change of electric characteristics, which may increase reliability of the memory device.

[0114]

Further, similar to the second embodiment, it is preferable that the film thickness of the insulating film under the charge retention film 242 (a portion of the silicon oxide film 241 on the offset region 271) is controlled to be constant, and further the film thickness of the insulating film disposed on the side face of the gate electrode (a portion of the silicon oxide film 241 in contact with the gate electrode 217) is controlled to be

constant. Consequently, the concentration of electric line of force generated by the electric charges stored in the silicon nitride film 242 may be roughly controlled, and leakage of electric charges may be prevented.

[0115]

(Fourth Embodiment)

This embodiment relates to optimization of the distance between a gate electrode, a memory function body, and a source/drain region.

[0116]

As shown in Fig. 14, reference symbol A denotes a gate electrode length in the cross section in channel length direction, reference symbol B denotes a distance (channel length) between source and drain regions, and reference symbol C denotes a distance from the edge of one memory function body to the edge of the other memory function body, more specifically a distance from the edge of a film (the side away from the gate electrode) having a function of holding the electric charges in one charge holding portion in the cross section in channel length direction to the edge of a film 242 (the side away from the gate electrode 217) having a function of holding the electric charges in the other memory function body 262.

[0117]

A relationship of B<C is preferable. When this

relationship is satisfied, in the channel region, there is present an offset region 271 between a portion under the gate electrode 217 and the source/drain regions 212, 213. By B<C, the electric charges stored in the memory function bodies 261, 262 (silicon nitride film 242) effectively change easiness of inversion in the entire part of the offset region 271. As a result, memory effect is increased, and high-speed read operation is particularly enabled.

[0118]

Also, when the gate electrode 217 and the source/drain regions 212, 213 are offset, that is, when the relationship of A<B is satisfied, easiness of inversion of the offset region when a voltage is applied to the gate electrode 217 is largely changed by an electric charge amount stored in the memory function bodies 261, 262. Consequently, memory effect increases and short channel effect can be reduced. However, as long as the memory effect is effective, the offset region is not necessarily required. Even when the offset region 271 is not present, if the impurity concentration in the source/drain regions 212, 213 is sufficiently small, the memory effect can still be effective in the memory function bodies 261, 262 (silicon nitride film 242).

[0119]

Therefore, the state of A<B<C is most

preferable.

[0120]

(Fifth Embodiment)

A memory device of semiconductor storage device according to this embodiment has essentially the same structure as that in the second embodiment except that the semiconductor substrate is SOI substrate as shown in Fig. 15.

[0121]

The memory device is structured such that an embedded oxide film 288 is formed on a semiconductor substrate 286, and on top of the embedded oxide film 288, SOI layer is further formed. In the SOI layer, there are formed diffusion regions 212, 213, and other areas constitute a body region 287.

[0122]

This memory device also brings about the functions and effects similar to those of the memory device in the second embodiment. Further, since the junction capacitance between the diffusion regions 212, 213 and the body region 287 may be considerably reduced, it becomes possible to increase a device speed and to decrease power consumption.

[0123]

(Sixth Embodiment)

A memory device in this embodiment has essentially the same structure as that in the second embodiment except that in the vicinity of the channel side of N type diffusion regions 212, 213, a P type highly-concentrated region 291 is added as shown in Fig. 16.

[0124]

More specifically, the concentration of P type impurity (e.g., boron) in the P type highly-concentrated region 291 is higher than the concentration of P type impurity in the region 292. An appropriate value of the P type impurity concentration in the P type highly-concentrated region 291 is, for example, around 5×10^{17} to 1×10^{19} cm^{-3}. Also, a value of the P type impurity concentration in the region 292 may be set to, for example, 5×10^{16} to 1×10^{18} cm^{-3}.

[0125]

Thus, providing the P type highly-concentrated region 291 makes the junction between the diffusion regions 212, 213 and the semiconductor substrate 211 steep right under the memory function bodies 261, 262. This facilitates generation of hot carriers in write and erase operation, thereby enabling reduction of voltage in write operation and erase operation or implementing high-speed write operation and erase operation. Further, since the impurity concentration in the region 292 is relatively small, a

threshold value when the memory is in erased state is small and so the drain current becomes large. Consequently, a read speed is increased. This makes it possible to provide a memory device having low rewrite voltage or a high rewrite speed, and having a high read speed.

[0126]

Also in Fig. 16, by providing the P type highly-concentrated region 291 in a position adjacent to the source/drain region and on the lower side of the memory function bodies 261, 262 (that is a position not right under the gate electrode), a threshold value of the entire transistor shows considerable increase. The degree of this increase is extremely larger than that in the case where the P type highly-concentrated region 291 is right under the gate electrode. When write electric charges (electrons in the case where the transistor is N channel type) are stored in the memory function bodies 261, 262, the difference becomes larger. When enough erase electric charges (positive holes in the case where the transistor is N channel type) are stored in the memory function body, a threshold value of the entire transistor is decreased down to a value determined by the impurity concentration in the channel region (region 292) under the gate electrode 217. More specifically, the threshold value in the erased state is not dependent on the impurity concentration in the P

type highly-concentrated region 291, whereas the threshold value in the written state receives extremely large influence. Therefore, disposing the P type highly-concentrated region 291 under the memory function bodies and adjacent to the source/drain region imparts extremely large fluctuation only to the threshold value in the written state, thereby enabling remarkable increase of memory effect (difference of threshold values in the erased state and the written state).

[0127]

(Seventh Embodiment)

A memory element in this embodiment has essentially the same structure as that in the second embodiment except that the thickness T1 of the insulating film 241 that separates the charge retention film (silicon nitride film 242) from the channel region or the well region 211 is smaller than the thickness T2 of the gate insulating film as shown in Fig. 17.

[0128]

The gate insulating film 214 has a lower limit of the thickness T2 because of the request for withstand voltage in memory rewrite operation. However, the thickness T1 of the insulating film 241 can be smaller than T2 regardless of the request for withstand voltage.

[0129]

In the memory device of the present embodiment, the thickness T1 of the insulating film has high design freedom as stated above because of the following reason. In the memory device of this embodiment, the insulating film that separates the charge retention film (silicon nitride) from the channel region or the well region is not interposed in between the gate electrode and the channel region or the well region. Consequently, the insulating film that separates the charge retention film (silicon nitride) from the channel region or the well region does not receive direct influence from the high-electric fields that affect in between the gate electrode and the channel region or the well region, but receives influence from relatively weak electric fields expanding from the gate electrode in lateral direction. As a result, despite the request for withstand voltage to the gate insulating film, it becomes possible to make T1 smaller than T2. Contrary to this, for example in EEPROM as typified by flash memory, an insulating film that separates a floating gate from the channel region or the well region is interposed in between a gate electrode (control gate) and the channel region or the well region, so that the insulating film receives direct influence from high electric fields of the gate electrode. In EEPROM, therefore, the thickness of the insulating film that separates the floating gate from the

channel region or the well region is limited, which hinders optimization of the functions of a memory device. As is apparent from the above description, the insulating film that separates the charge retention film (silicon nitride) from the channel region or the well region is not interposed in between the gate electrode and the channel region or the well region, which is the essential reason why the design freedom of T1 is enhanced.

[0130]

Decreasing the thickness T1 of the insulating film facilitates injection of electric charges into the memory function bodies, decreases voltage for write operation and erase operation, or enables high-speed write operation and erase operation. In addition, since an electric charge amount induced in the channel region or the well region increases when electric charges are stored in the silicon nitride film, increased memory effect may be implemented.

[0131]

Some electric lines of force having short length in the memory function body do not pass the silicon nitride film 242 as shown with an arrow 284 in Fig. 13. Since electric field strength is relatively large on such a short electric line of force, the electric fields along the electric line of force play an important role in rewrite

operation. By decreasing the thickness T1 of the insulating film 241, the silicon nitride film 242 moves to the lower side of the Fig. 13, so that the electric line of force shown with the arrow 283 passes the silicon nitride film 242. As a consequence, an effective dielectric constant in the memory function body along the electric line of force 284 in the direction of arrow 284 becomes large, which makes it possible to make potential difference between the both ends of the electric line of force 284 smaller. Therefore, most part of voltage applied to the gate electrode 217 is used to strengthen the electric fields in the offset region, thereby implementing high-speed write operation and erase operation.

[0132]

As is clear from the above, by setting the thickness T1 of the insulating film 241 and the thickness T2 of the gate insulating film 214 as T1<T2, it becomes possible to decrease voltage in write operation and erase operation or implement high-speed write operation and erase operation, and to enable further increase of memory effect without degrading withstand voltage capability of the memory.

[0133]

It is noted that the thickness T1 of the insulating film is preferably 0.8nm or more, that is the

limit range in which uniformity in manufacturing process or certain level of film quality may be maintained and holding characteristics do not suffer extreme deterioration.

[0134]

More specifically, in the case of liquid crystal driver LSI which has a severe design rule and requires high withstand voltage, maximum 15 to 18V voltage is necessary for driving liquid crystal panel TFT (Thin Film Transistor). Eventually, it is not possible to make the gate oxide film thinner. In the case of mounting a nonvolatile memory of the present invention as an image adjuster together with other devices on the liquid crystal driver LSI, the memory device of the present invention enables optimum design of the thickness of the insulating film that separates the charge retention film (silicon nitride film 242) from the channel region or the well region independently of the thickness of the gate insulating film. For example, in a memory cell with a gate electrode length (word line width) of 250nm, there may be separately set like T1=20nm and T2=10nm, fulfilling a memory cell with good write efficiency. (Short channel effect is not generated even though T1 is larger than that of normal logic transistors, because the source/drain region is offset from the gate electrode.)

[0135]

(Eighth Embodiment)

A memory device according to this embodiment has essentially the same structure as that in the second embodiment except that the thickness (T1) of the insulating film that separates the charge retention film (silicon nitride film 242) from the channel region or the well region is larger than the thickness (T2) of the gate insulating film as shown in Fig. 18.

[0136]

The gate insulating film 214 has an upper limit of the thickness T2 because of the request for prevention of short channel effect of the device. However, the thickness T1 of the insulating film 241 can be larger than T2 regardless of the request for prevention of short channel effect. More specifically, as miniaturization scaling proceeds (thinning of the gate insulating film proceeds), the thickness of the insulating film that separates the charge retention film (silicon nitride film 242) from the channel region or the well region may be optimally designed independently of the thickness T2 of the gate insulating film, which implements the effect that the memory function body will not disturb scaling.

[0137]

In the memory device of the present embodiment, the thickness T1 of the insulating film has high design

freedom as stated above because, as is already described, the insulating film that separates the charge retention film from the channel region or the well region is not interposed in between the gate electrode and the channel region or the well region. As a result, despite the request for prevention of short channel effect to the gate insulating film, it becomes possible to make T1 larger than T2.

[0138]

Increasing the thickness of T1 makes it possible to prevent dissipation of the electric charges stored in the memory function body and to improve holing characteristics of the memory.

[0139]

Therefore, setting as T1>T2 enables improvement of holding characteristics without deteriorating short channel effect of the memory. It is noted that the thickness T1 of the insulating film is preferably 20nm or less in consideration of reduction of a rewrite speed.

[0140]

More specifically, a conventional nonvolatile memory as typified by flash memory is structured such that a selection gate electrode constitutes a write/erase gate electrode, and a gate insulating film (including a floating gate) corresponding to the write/erase gate electrode

serves also as an electric charge storage film. Consequently, since the request for miniaturization (creation of thinner devices is essential for restraining short channel effect) conflicts the request for securing reliability (in order to control leakage of stored electric charges, the thickness of an insulating film that separates a floating gate from the channel region or the well region cannot be decreased to smaller than approx. 7nm), miniaturization of the device is difficult. In fact, according to ITRS (International Technology Roadmap for Semiconductors), miniaturization of a physical gate length down to approx. 0.2 micron or lower is not yet in sight. In the memory device of the present invention, independent designing of T1 and T2 is available as described above, and therefore miniaturization becomes possible. For example, in a memory cell with a gate electrode length (word line width) of 45nm, there is separately set like T2=4nm and T1=7nm, fulfilling a semiconductor storage device free from generation of short channel effect. Short channel effect is not generated even though T2 is set larger than that of normal logic transistors, because the source/drain region is offset from the gate electrode. Also, since the source/drain region is offset from the gate electrode in the memory device of the present invention, miniaturization is further facilitated compared to normal logic transistors.

[0141]

Summarizing the above description, since an electrode for supporting write and erase operation is not present above the memory function body, the insulating film that separates the charge retention film from the channel region or the well region does not directly receive the influence of high electric fields that affect in between the electrode that supports write and erase operation and the channel region or the well region, but receives influence only from relatively weak electric fields expanding from the gate electrode in lateral direction. This makes it possible to fulfill a memory cell having the gate length miniaturized more than the gate length of the logic transistors in comparison with the same processing accuracy.

[0142]

(Ninth Embodiment)

This embodiment relates to changes of electric characteristics when rewrite operation is performed in the memory device.

[0143]

Fig. 19 is a view showing characteristic curves of a drain current (Id) versus a gate voltage (Vg) (measured values) where an electric charge amount in the memory function body of an N-channel type memory device

varies between erase state and written state. As clearly shown in Fig. 19, when write operation is performed in the erased state (a solid line), as shown by a broken line, not only the threshold value simply rises, but inclination of the graph dramatically falls especially in sub-threshold region. Therefore, even in the region with relatively high gate voltage (Vg), a drain current ratio of the erased state to the written state is large. For example in the point of Vg=2.5V, the current ratio is still two digits or more. This characteristic is largely different from that in the case of a flash memory shown in Fig. 22.

[0144]

The appearance of the above characteristic in the memory device is a phenomenon peculiar to the case where the gate electrode and the diffusion region are offset and therefore the gate electric fields are difficult to reach the offset region. When the memory device is in the written state, an inversion layer is extremely difficult to be generated in the offset region below the memory function body even if a positive voltage is applied to the gate electrode. This causes smaller inclination of the Id-Vg curve line in the sub-threshold region in the written state. When the memory device is in the erased state, high-density electrons are induced in the offset region. Further, when 0V is applied to the gate electrode

(i.e., in OFF state), electrons are not induced in the channel below the gate electrode (and therefore an off current is small). This causes large differential coefficient of the Id-Vg curve line in the sub-threshold region in the erased state and a large increase rate of current (conductance) even in the voltage region over the threshold.

[0145]

As is clear from the above description, the memory device of the semiconductor storage device according to the present invention makes it possible to make the drain current ratio of the erased state to the written state particularly large.

[0146]

(Tenth Embodiment)

A portable telephone as portable electronic equipment, in which the semiconductor storage device is incorporated, is shown in Fig. 20.

[0147]

This portable telephone is constituted essentially of a control circuit 511, a battery 512, an RF (Radio Frequency) circuit 513, a display section 514, an antenna 515, a signal line 516 and a power line 517. A semiconductor storage device 511a according to any one of the foregoing embodiments is incorporated in the control

circuit 511. The control circuit 511 should preferably be an integrated circuit where devices of an identical structure are concurrently used as memory circuit elements and logic circuit elements. This facilitates the manufacturing of integrated circuits and allows the manufacturing cost of the portable electronic equipment to be especially reduced.

[0148]

As described above, by employing the semiconductor storage device that facilitates the fabricating process for the memory section and the logic circuit section in combination, that is easy to miniaturize, and that allows a high speed read operation for the portable electronic equipment, it is possible to improve the reliability and operating speed of the portable electronic equipment, reduce the size of the portable electronic equipment, and reduce the production costs.

[0149]

Effect of the invention:

As is apparent from the above description, according to the semiconductor storage device of the first invention, the memory function bodies are formed independently of the gate insulating film and provided on both sides of the gate electrode. Thus, the device is able to perform a two-bit operation. Furthermore, because the

memory function bodies are separated from each other by the gate electrode, interference during rewrite can effectively be prevented. Further, because the gate insulating film is independent of the memory function bodies, the gate insulating film is made thinner, so that short channel effect can be easily prevented. Thus, further miniaturization of a memory element is facilitated.

[0150]

The semiconductor storage device of the second invention correspondes to an embodiment of an array of a plurality of the semiconductor storage devices of the first invention. Therefore, miniaturization of the semiconductor storage device comprising the memory elements that are arrayed is easier.

[0151]

The semiconductor storage device of the third invention also corresponds to an embodiment of an array of a plurality of the semiconductor storage devices of the first invention. Further, the memory function bodies are formed of one or more insulative materials and arranged only on both sides of the single word line. Therefore, the fabrication process for the semiconductor stsorage device having the memory elements arrayed is simplified, which in turn provides improved yields. Further, miniaturization of the memory elements is easier, so that the scale of

integration will be increased. In addition, the write operation is well performed.

[0152]

In one embodiment, since a word line to be selected when information is rewritten to the memory element is only the single word line, the number of word lines that are required for the memory operations is made minimum. Thus, a memory cell array can be packed at a higher density.

[0153]

According to the semiconductor storage device of the fourth invention, the memory function bodies are comprised of one or more insulative materials and formed on both sides of the single gate electrode such that at least part of each memory function body overlaps with part of the corresponding diffusion region. Therefore, the fabrication process of the memory element is simplified and thus increase yields. Further, miniaturization of the memory elements is easier, and the write operation to the memory elements is well performed.

[0154]

In one embodiment, since the semiconductor layer is comprised of a SOI layer, junction capacitance between the diffusion regions and a body region is markedly reduced, which enables the increase of the operation speed

of the memory elements and the reduction of power consumption.

In one embodiment, since the semiconductor layer includes a well region, it is easy to controll electric characteristics (breakdown voltage, junction capacitance, short-channel effect), with the impurity concentration in an area right under the gate insulation film being made optimum in view of the memory operations (rewrite operations and read operations).

[0155]

In one embodiment, since each of the memory function bodies includes a charge retention film having a function of storing electric charges, and an insulation film. In this embodiment, it is possible to prevent dissipation of electric charges and improve the memory retention characteristic. Also, it is possible to properly reduce the volume of the charge retention film, as compared with a case in which the memory function body consists of the charge retention film only. Further, the proper reduction of the volume of the charge retention film can restrain migration of the electric charges within the charge retention film, thus suppressing a change in characteristics due to the migration of the charges during the memory retention. Thus, an improved memory retention characteristic is achieved.

[0156]

In one embodiment, since the memory function body includes a charge retention film having a surface roughly parallel to a surface of the gate insulation film, it is possible to effectively control easiness of formation of an inversion layer in the offset region with use of an amount of electric charges stored in the charge retention film, thereby enabling increase of memory effect. Because the charge retention film is substantially parallel to the surface of the gate insulation film, change of memory effect may be kept relatively small even with a dispersed offset amount, enabling restraint of memory effect dispersion. In addition, because the charge retention film is in the shape of a film substantially parallel to the surface of the gate insulation film, upward movement of electric charges is suppressed, and therefore change of characteristics due to the movement of electric charges during memory holding is restrained. Thus, it is possible to obtain a semiconductor storage device having good charge holding characteristics wherein the memory effect is large and less varied.

[0157]

In one embodiment, since the memory function body includes a charge retention film extended roughly parallel to a side surface of the gate electrode or the

word line, the holding characteristic of the device is prevented from deterioration, and at the same time, the rewriting speed can be increased.

[0158]

In one embodiment, since the memory function body further includes an insulation film that separates the gate electrode or the word line from the charge retention film extended roughly parallel to the side surface of the gate electrode or the word line, movement of the electric charges between the gate electrode and the charge retention film extended roughly parallel to the gate electrode side surface is suppressed. Thus, reliability of the semiconductor storage device increases.

[0159]

In one embodiment, since the memory function body further includes an insulation film that separates the charge retention film including a surface roughly parallel to the surface of the gate insulating film from the channel region or the semiconductor layer, dissipation of charges from the first portion of the charge retention film is suppressed. Therefore, a semiconductor storage device with better holding characteristics is obtainable.

[0160]

In one embodiment, since the insulation film that separates the the charge retention film from the

channel region or the semiconductor layer has a film thickness, which is smaller than a film thickness of the gate insulation film and not smaller than 0.8 nm, without deteriorating the voltage withstanding performance or electric strength of the memory, reduction of voltage in the write operation and erase operation or implementing a high-speed write operation and erase operation is enabled. This makes it possible to increase memory effect.

[0161]

In one embodiment, since the insulation film that separates the charge retention film from the channel region or the semiconductor layer has a film thickness, which is greater than a film thickness of the gate insulation film and not greater than 20 nm, it is possible to improve the holding characteristics without deteriorating the memory short channel effect.

[0162]

Portable electronic equipment of the fifth invention includes the semiconductor storage device of the present invention. Since the semiconductor storage device that facilitates the fabricating process for the memory section and the logic circuit section in combination, and that allows a high speed read operation, is employed for the portable electronic equipment, it is possible to improve the operating speed of the portable electronic

equipment, and reduce the production costs.

Brief explanation of the drawings:

Fig. 1 is a schematic sectional view of an essential part of a memory element (First Embodiment) of the present invention.

Fig. 2 is a schematic sectional view of an essential part of a modification of the memory element (First Embodiment) of the present invention.

Fig. 3 is a view for explaining the write operation of the memory element (First embodiment) of the present invention.

Fig. 4 is a view for explaining the write operation of the memory element (First embodiment) of the present invention.

Fig. 5 is a view for explaining the erase operation of the memory element (First embodiment) of the present invention.

Fig. 6 is a view for explaining the erase operation of the memory element (First embodiment) of the present invention.

Fig. 7 is a view for explaining the read operation of the memory element (First Embodiment) of the present invention.

Fig. 8 is a schematic sectional view of an essential part of a memory element (Second Embodiment) of

the present invention.

Fig. 9 is an enlarged schematic sectional view of the essential part of Fig. 8.

Fig. 10 is an enlarged schematic sectional view of an essential part of a modification of Fig. 8.

Fig. 11 is a graph showing the electrical characteristic of the memory element (Second Embodiment) of the present invention.

Fig. 12 is a schematic sectional view of an essential part of a modification of the memory element the memory element (Second Embodiment) of the present invention.

Fig. 13 is a schematic sectional view of an essential part of a memory element (Third Embodiment) of the present invention.

Fig. 14 is a schematic sectional view of an essential part of a memory element (Fourth Embodiment) of the present invention.

Fig. 15 is a schematic sectional view of an essential part of a memory element (Fifth Embodiment) of the present invention.

Fig. 16 is a schematic sectional view of an essential part of a memory element (Sixth Embodiment) of the present invention.

Fig. 17 is a schematic sectional view of an essential part of a memory element (Seventh Embodiment) of

the present invention.

Fig. 18 is a schematic sectional view of an essential part of a memory element (Eighth Embodiment) of the present invention.

Fig. 19 is a graph showing the electrical characteristic of a memory element (Ninth Embodiment) of the present invention.

Fig. 20 is a schematic construction view of portable electronic equipment (Tenth Embodiment) in which the semiconductor storage device of the present invention is incorporated.

Fig. 21 is a schematic sectional view of an essential part of a flash memory as a prior art.

Fig. 22 is a graph showing the electrical characteristic of the conventional flash memory as the prior art.

Explanation of the numerals:

101: semiconductor substrate

102: P-type well region

103: gate insulation film

104: gate electrode

105, 131: memory function body

107: diffusion region

109, 113: silicon nitride film

111, 112: silicon nitride film

120: offset region

121: region located under gate electrode

Document name: Drawings

Fig. 1

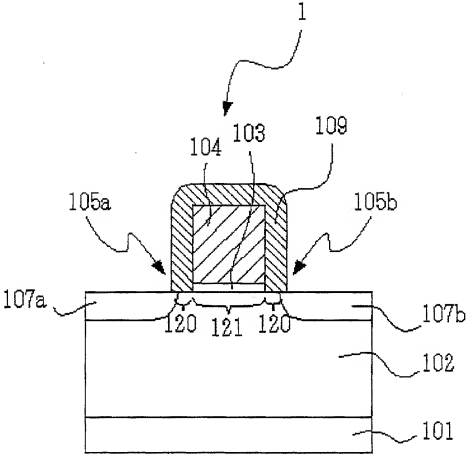
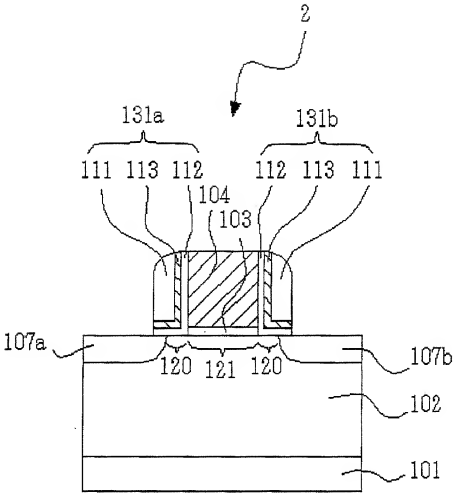


Fig. 2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107b
102
101

Fig. 3

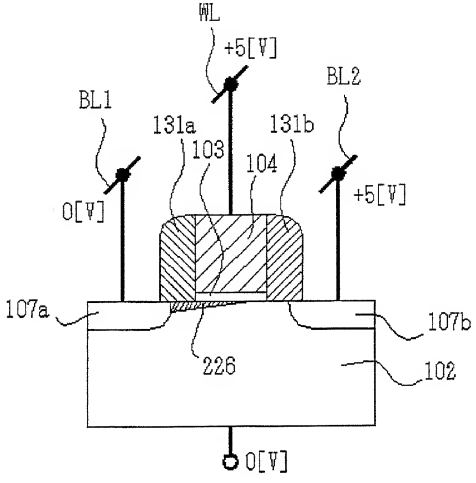


Fig. 4

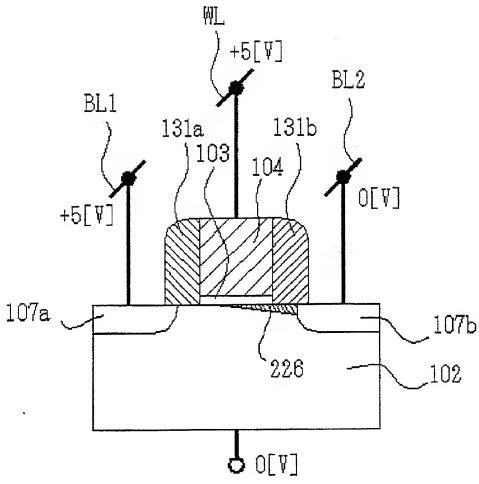


Fig. 5

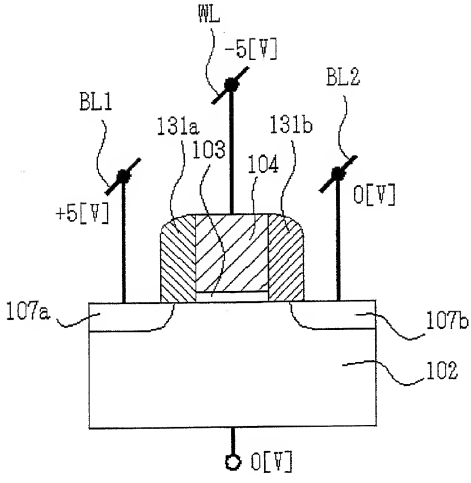


Fig. 6

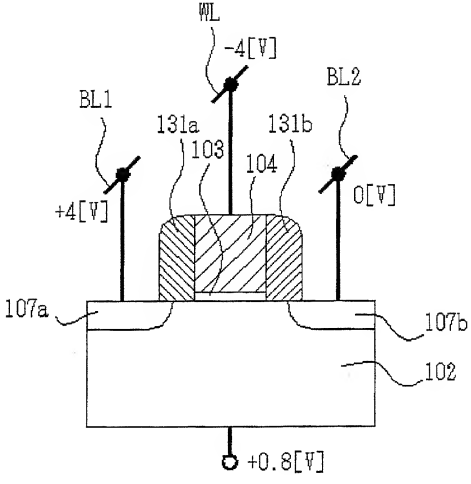
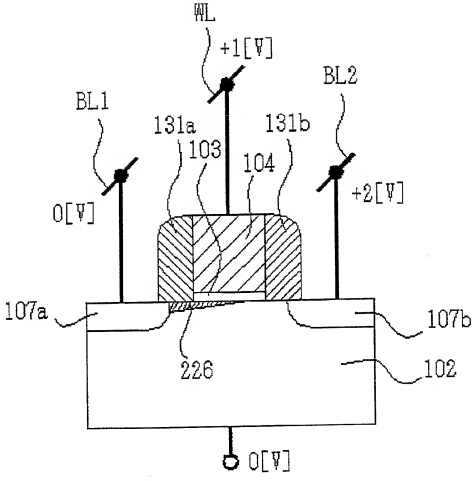


Fig. 7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BL2
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Fig. 8

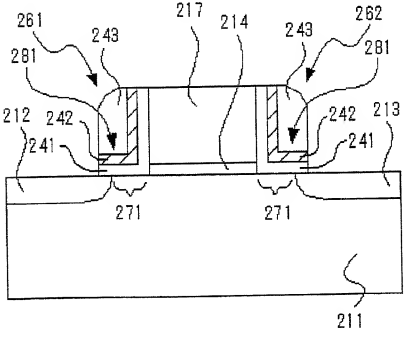
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Fig. 9

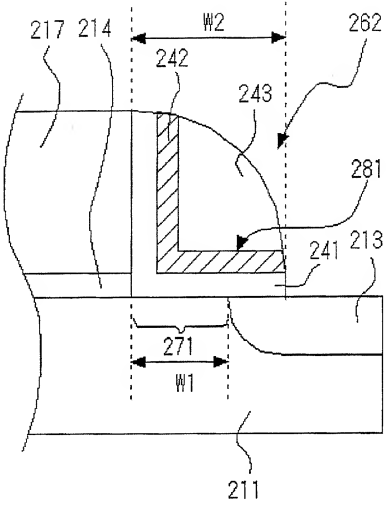


Fig. 10

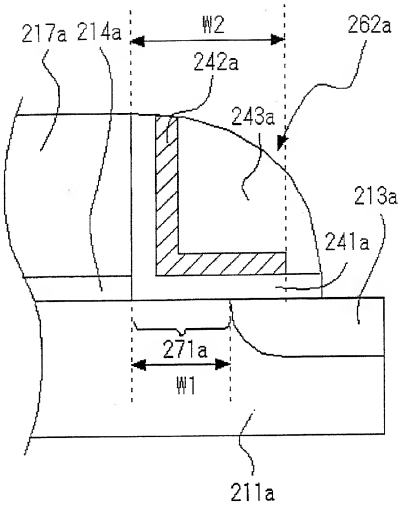
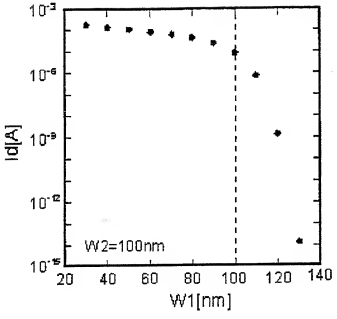


Fig. 11



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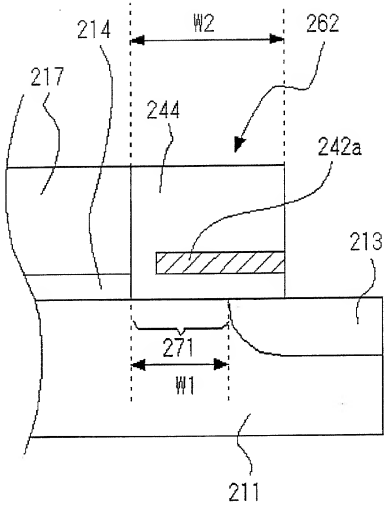


Fig. 13

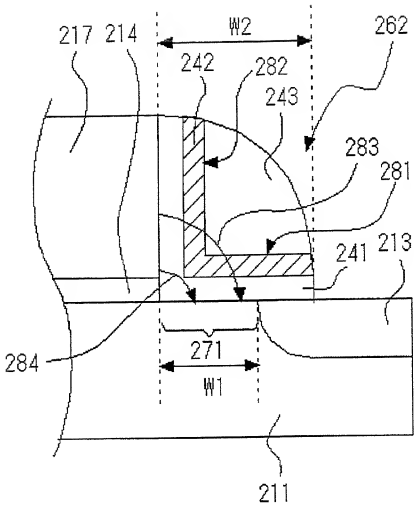
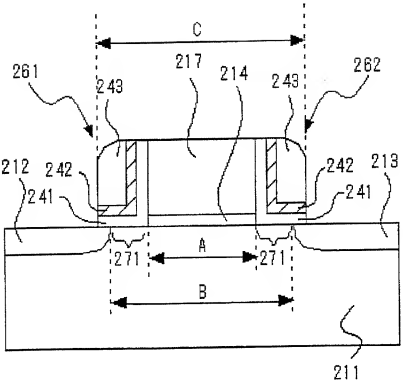


Fig. 14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B
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Fig. 15

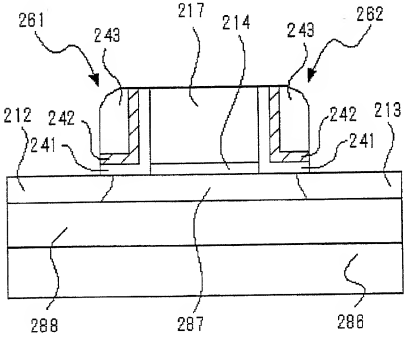
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Fig. 16

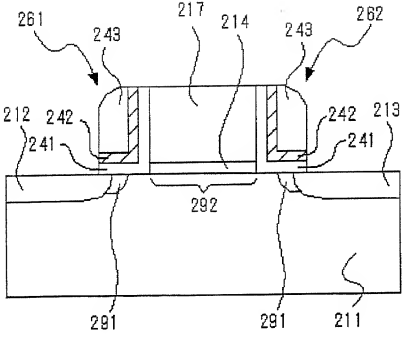
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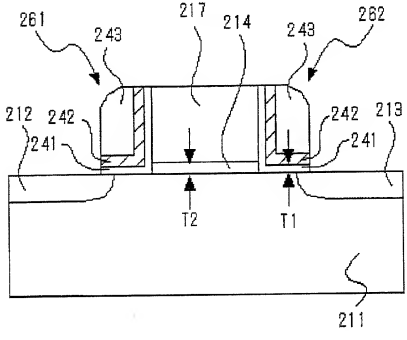
Fig. 17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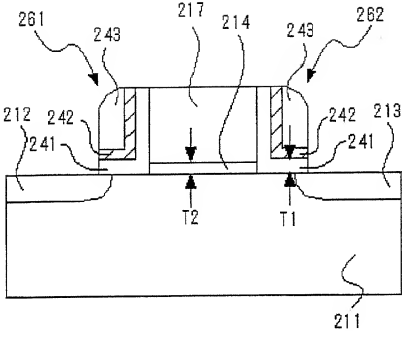
T2
T1
211

Fig. 18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T2
T1
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Fig. 19

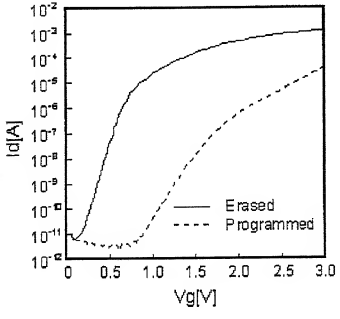
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Fig. 20

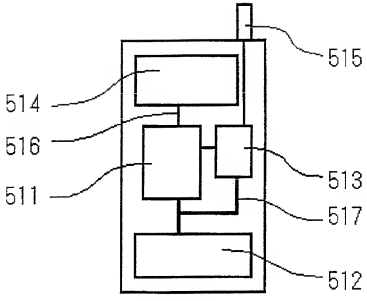


Fig. 21

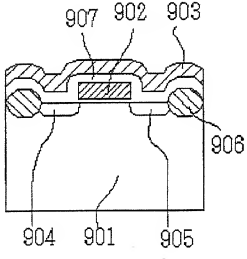
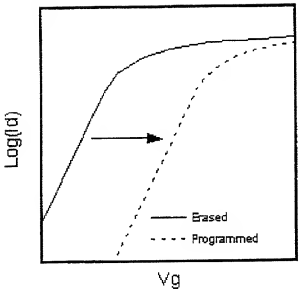


Fig. 22



Document name: Abstract

Summary:

Object: To provide a non-volatile memory in which two-bit operations are possible and miniaturization is facilitated.

Means of solution: By the arrangement comprising: a single gate electrode formed on a semiconductor layer, with a gate insulation film disposed therebetween; a channel region arranged under the gate electrode; diffusion regions arranged on opposite sides of the channel region; and memory function bodies formed at least on opposite sides of the gate electrode and having a function to retain electric charges, 2-bit operations are possible because the memory function bodies are formed on both sides of the gate electrode, independently of the gate insulation film. Further, because the memory function bodies are each separated from each other by the gate electrode, interference during rewrite operation is effectively suppressed. Also, short-channel effect is suppressed through thinning of the gate insulation film. Miniaturization of memory elements is thus facilitated.

Selected figure: Fig. 1